IN THE CLAIMS

Please amend the claims as follows:

6.(Twice Amended) The transistor of claim 1, wherein ~~the~~ silicon carbide gate material [is described by] comprises ~~$Si_{1-X}C_X$ and X~~ is approximately less than or equal to 0.5.

11.(Amended) An integrated circuit device comprising:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate [adjacent to] over the channel region and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate [adjacent to] over the channel region and separated therefrom by an insulating layer.

14.(Amended) The integrated circuit device of claim 11, wherein the insulating layers, which separate the silicon carbide gates in each of the n-channel and p-channel transistors from their respective channel regions, are comprised of silicon [oxide] dioxide.

23.(Amended) The [semiconductor memory] integrated circuit device of claim 11 wherein each silicon carbide gate comprises ~~$Si_{1-X}C_X$ and X~~ is approximately less than or equal to 0.5.

25.(Amended) The semiconductor memory device of claim 15 wherein pairs of the transistors in the memory array comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor

including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate [adjacent to] over the channel region and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate [adjacent to] over the channel region and separated therefrom by an insulating layer.

27.(Amended) The semiconductor memory device of claim 15 wherein the silicon carbide [gate] material comprises polycrystalline silicon carbide.

28.(Amended) The semiconductor memory device of claim 15 wherein the silicon carbide [gate] material comprises microcrystalline silicon carbide.

29.(Amended) The semiconductor memory device of claim 15 wherein the [silicon carbide] gate is separated from the semiconductor surface layer by an insulating layer of silicon [oxide] dioxide.

30.(Amended) The semiconductor memory device of claim 15 ~~wherein the [silicon carbide]~~ gate comprises $Si_{1-X}C_X$ and X is approximately less than or equal to 0.5.

31.(Amended) A semiconductor memory device comprising:

a memory array including a plurality of transistors wherein pairs of the transistors comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate [adjacent to] over the channel region and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate [adjacent to] over the channel region and separated therefrom by an insulating layer;

addressing circuitry [for addressing] to address the memory array; and

control circuitry [for controlling] to control read, write, and erase operations of the memory device.

35. (Twice Amended) The semiconductor memory device of claim 31 wherein each insulating layer comprises silicon [oxide] dioxide.

Please add the following new claims:

37.(New) A transistor comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising a p+ doped silicon carbide compound SiC on the insulating layer.

38.(New) The transistor of claim 37 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound SiC comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide; and

the silicon carbide compound SiC is p+ doped with boron.

39.(New) The transistor of claim 37 wherein:

the substrate comprises p-type silicon;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

40.(New) The transistor of claim 37 wherein:

the substrate comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

41.(New) A transistor comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising an n+ doped silicon carbide compound SiC on the insulating layer.

42.(New) The transistor of claim 41 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound SiC comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide; and

the silicon carbide compound SiC is n+ doped with phosphorus.

43.(New) The transistor of claim 41 wherein:

the substrate comprises p-type silicon;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

44.(New) The transistor of claim 41 wherein:

the substrate comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

45.(New) A transistor comprising:

a semiconductor surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the semiconductor surface layer;

an insulating layer on the semiconductor surface layer over the channel region; and

a gate comprising a silicon carbide compound Si_xC_{1-x} on the insulating layer wherein x is less than 0.5.

46.(New) The transistor of claim 45 wherein:

the semiconductor surface layer comprises p-type silicon;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound Si_xC_{1-x} comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

47.(New) The transistor of claim 45 wherein:

the semiconductor surface layer comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

48.(New) The transistor of claim 45 wherein the silicon carbide compound Si_xC_{1-x} is p+ doped with boron or n+ doped with phosphorus.

49.(New) The transistor of claim 45 wherein:

the gate comprises a floating gate; and

the transistor further comprises a polysilicon control gate separated from the floating gate by an intergate dielectric comprising oxide.

50.(New) A transistor comprising:

a semiconductor surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the semiconductor surface layer;

an insulating layer on the semiconductor surface layer over the channel region; and

a gate comprising a silicon carbide compound Si_xC_{1-x} on the insulating layer wherein x is greater than 0.5.

51.(New) The transistor of claim 50 wherein:

the semiconductor surface layer comprises p-type silicon;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound Si_xC_{1-x} comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

52.(New) The transistor of claim 50 wherein:

the semiconductor surface layer comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

53.(New) The transistor of claim 50 wherein the silicon carbide compound Si_xC_{1-x} is p+ doped with boron or n+ doped with phosphorus.